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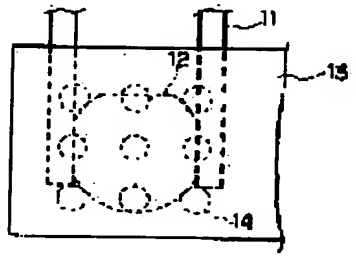
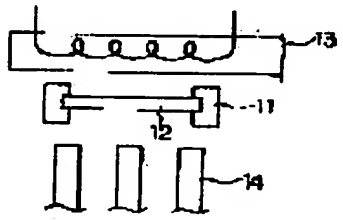
(54) MANUFACTURE OF SEMICONDUCTOR DEVICE

(57)Abstract:
PURPOSE: To achieve that impurities are hard to be left on a treated surface, that the treated surface is hard to damage, that the impurities are hard to diffuse and that an element characteristic is hard to deteriorate by a method wherein the following are executed simultaneously or alternately: a process wherein a substrate to be treated is heated for a short time by a rapid thermal annealing method; and a process wherein the beam of the constituent substance of the substrate to be treated is irradiated.
CONSTITUTION: A substrate holder 11 has a shape which sandwiches edges of a substrate 12 in such a way that the surface on the side of an element formation region on the substrate 12 and the rear on its opposite side are not covered; the substrate 12 is arranged in such a way that its surface is faced downward; an infrared lamp 13 which can irradiate the rear is provided. Three × three pieces of molecular-beam cells 14 are arranged in a direction perpendicular to the surface of the substrate 12; the surface of the substrate 12 can be irradiated uniformly with molecular beams. The molecular beams are charged with high-purity Si. The Gi substrate 12 is moved between the infrared lamp 13 and the molecular-beam cells 14; its surface temperature is held at about 300° C by the infrared lamp 13; the temperature of the molecular-beam cells 14 is raised to about 1400° C; the temperature of the substrate 12 is raised and it is lowered immediately after the molecular beams have been irradiated.



(a)



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CLAIMS

[Claim(s)]
[Claim 1] a processed substrate — RTA (Rapid Thermal Annealing) — the manufacture approach of the semiconductor device characterized by including the process which performs surface treatment of this processed substrate by performing to coincidence the heating process which carries out short-time heating by law, and the beam exposure process which irradiates the beam of the constituent of this processed substrate at this processed substrate, or carrying out by a unit of at least 1 time by turns.
[Claim 2] It is the manufacture approach of the semiconductor device according to claim 1 characterized by performing said beam exposure by two or more molecular-beam cels.
[Claim 3] Said heating is the manufacture approach of the semiconductor device according to claim 1 to 2 characterized by being infrared exposure heating.
[Claim 4] It is the manufacture approach of the semiconductor device according to claim 3 characterized by performing said infrared exposure heating from the rear face of the opposite side of the component formation field of said processed substrate, and performing this beam exposure from the front face by the side of the component formation field of this processed substrate in case said heating process and said beam exposure stroke are performed to coincidence.
[Claim 5] It is the manufacture approach of the semiconductor device according to claim 3 characterized by performing said infrared exposure heating and this beam exposure process from the field by the side of the component formation field of said processed substrate in case said heating process and said beam exposure process are performed by turns.
[Claim 6] Said surface treatment process is the manufacture approach of the semiconductor device according to claim 5 characterized by being pretreatment before membrane formation.
[Claim 7] Said pretreatment is the manufacture approach of the semiconductor device according to claim 6 characterized by being pretreatment in the multi chamber equipment which has two or more chambers.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] In case this invention can relate to the manufacture approach of a semiconductor device, can be applied to the surface treatment approach of substrates, such as silicon used for a semiconducting crystal manufacturing technology and an electron device manufacture process, in detail and removes the natural oxidation film of a processed substrate especially, impurity residue, a damage, etc. are made hard to produce on a processing front face, and it relates to the manufacture approach of the semiconductor device which degradation of a component property can be made hard to produce.
[0002] In recent years, development research of the basic technique is actively performed towards implementation of ULSI integrated circuits, such as 256Mb and DRAM of 1Gb class. And the minimum processing dimension Ruhr in the integrated circuit of this class It is very as small as 0.3 micrometers or less, and, moreover, quality improvement is demanded with low temperature-ization in each process. And a processing process is also changing a lot with the demand of high integration of a component.
[0003]
[Description of the Prior Art] Drawing 7 is drawing showing the bad influence which the natural oxidation film on the front face of silicon has on device basic structure. It is SiO2 after the natural oxidation film 32 has arisen on silicon substrate 31 front face, as shown in drawing 7 (a). It is SiO2 when sequential formation of an insulator layer 33 and the Pori Si wiring layer 34 is carried out. Gas, an impurity, etc. are spread in an insulator layer 33 and the Pori Si wiring layer 34, and it is SiO2. The membraneous quality of an insulator layer 33 and the Pori Si wiring layer 34 worsens, and a component [become / easy to produce a poor proof pressure] property becomes easy to deteriorate.
[0004] Moreover, it is SiO2 after the natural oxidation film 32 has arisen on silicon substrate 31 front face, as shown in drawing 7 (b). It is SiO2 when sequential formation of an insulator layer 33 and the aluminum wiring layer 34 is carried out. Gas, an impurity, etc. are spread in an insulator layer 33 and the aluminum wiring layer 34, and it is SiO2. The membraneous quality of an insulator layer 33 and the aluminum wiring layer 34 worsens, and component properties, — induction of the defect is carried out into the aluminum wiring layer 34 — become easy to deteriorate.
[0005] Moreover, it is SiO2 as shown in drawing 7 (c). After the natural oxidation film 32 has arisen, the Pori Si wiring layer 34 is formed in silicon substrate 31 front face in opening 33a formed in the insulator layer 33. Furthermore, if the SiN insulator layer 35 is formed in this Pori Si wiring layer 34 front face after the natural oxidation film has arisen Gas, an impurity, etc. are spread in the Pori Si wiring layer 34 and the SiN insulator layer 35, and the membraneous quality of the Pori Si wiring layer 34 and the SiN insulator layer 35 worsens. That it is easy to produce poor contact in a silicon substrate 31 and the Pori Si wiring layer 34, it becomes, or capacitor capacity falls, it becomes easy to produce a defect, and a component property becomes easy to deteriorate. Especially the problem in this drawing 7 is. It becomes remarkable in the process of the ULSI integrated circuit of 0.3-micrometer level etc.
[0006] Thus, by the former, since the component property deteriorated after the natural oxidation film had arisen and forming the following layer, before forming membranes, surface treatment was carried out by argon sputter etching, hydrogen plasma etching or fluorine radical etching, etc., and the dirt of the natural oxidation film had been removed.
[0007]
[Problem(s) to be Solved by the Invention] however, by the manufacture approach of the above-mentioned

conventional semiconductor device Since surface treatment was carried out by argon sputter etching, hydrogen plasma etching or fluorine radical etching, etc., After impurities, such as hydrogen and a fluorine, tended to remain on a processing front face and the impurity had remained, when the following layer was formed, there was a problem that the membraneous quality of the film which the above-mentioned impurity was spread in the formed film, consequently was formed worsened, and a component property tends to deteriorate. Moreover, since surface preparation was carried out by etching, there was a problem that a damage tends to go into a processing front face. When the damage went into the front face, surface morphology worsened and a diffusion layer was in a substrate, it might etch to the diffusion layer.

[0008] For this reason, an impurity remains on a processing front face, in order to solve the problem that a damage will go into a processing front face, a heating furnace is used, heating at high temperature of the silicon processed substrate is carried out at about 1000 degrees C, and the method of removing the SiO2 natural-oxidation film is learned for the former by irradiating Si beam for about ten seconds further. In addition, it does not pretreat to a silicon substrate but is SiO2. When removing the natural oxidation film, substrate temperature can be made into about 1000 degrees C, and a pure substrate front face can be obtained by irradiating Si beam for about ten seconds.

[0009] However, by this approach, since the temperature up of the furnace was used and carried out to the elevated temperature of 1000 degrees C raising substrate temperature, a heating up time will take long duration. For this reason, diffusion of impurities, such as a diffusion layer of a component formation field, arose for the elevated-temperature maintenance in this long duration, and there was a problem that the component property accompanying impurity diffusion will deteriorate similarly with having described above, after all.

[0010] So, in this invention, in case the natural oxidation film of a processed substrate front face is removed, while being able to make impurity residue hard to produce on a processing front face, it can be made hard to go a damage into a processing front face, and impurity diffusion can be made hard to produce moreover and it aims at offering the manufacture approach of the semiconductor device which degradation of a component property can be made hard to produce.

[0011]

[Means for Solving the Problem] the manufacture approach of the semiconductor device by this invention — the above-mentioned purpose achievement sake — a processed substrate — RTA (Rapid Thermal Annealing) — the process which performs surface treatment of this processed substrate is included by performing to coincidence the heating process which carries out short-time heating by law, and the beam exposure process which irradiates the beam of the constituent of this processed substrate at this processed substrate, or carrying out by a unit of at least 1 time by turns.

[0012] Substrates, such as Si, GaAs, and InP, are mentioned to the processed substrate concerning this invention, and beams, such as Si, As, and P, are mentioned to the beam of the constituent of the processed substrate to this. Moreover, infrared exposure heating etc. is mentioned to heating by the RTA method. A processed substrate can be irradiated with distribution equally more sufficient than the case where it carries out in a molecular-beam cel single by the case where said beam exposure is performed by two or more molecular-beams cel in this invention being desirable, and arranging [as opposed to / in this case / a processed substrate] a molecular-beam cel with equally sufficient suitably distribution.

[0013] In this invention, in case a heating process and a beam exposure process are performed to coincidence For example, an infrared exposure line etc. is heated from a processed substrate rear face (field of a component formation field and the opposite side). That what is necessary is just made to perform a beam exposure from a processed substrate front face (field by the side of a component formation field), in case a heating process and a beam exposure process are performed by turns, what is necessary is just made to perform heating and a beam exposure of an infrared exposure etc. by turns from a processed substrate front face. While being able to simplify a process defined system rather than the case of the latter, surface treatment of the case of the former can be carried out easily. In the case of the latter, since both processes can be performed from the front-face side of a processed substrate, dispersion in substrate skin temperature can be made fewer than the case of the former.

[0014] this invention — setting — wiring of aluminum etc., and SiO2 etc. — it can be made to be able to apply to pretreatment before membrane formation of an insulator layer etc. preferably, and can be made to apply to the head end process in multi chamber equipments which have two or more chambers, such as CVD and a sputtering system, preferably especially

[0015]

[Function] Since the temperature up of the substrate temperature was carried out at the furnace in the former as mentioned above, as shown in drawing 1 (a) If long duration will be needed by the time it amounts to 1000 degrees C which is the target temperature, and it is only for about ten seconds about the temperature of 1000 degrees C in fact, although the natural oxidation film is removable Since a substrate will be put from several minutes to the bottom of the elevated temperature of the long duration of dozens of minutes, diffusion and the damage of an impurity started and there was a problem practically.

[0016] on the other hand — this invention — RTA — that about several seconds should just be to carry out a temperature up to 1000 degrees C as shown in drawing 1 (b) since law is used, since it is good also for a temperature fall in about dozens of seconds from several seconds, the time amount which is maintaining the substrate at the elevated temperature is very shorter than the case where the conventional furnace is used, and ends. Since this can make a process finish before the effect by diffusion of an impurity appears, it can be said to be a low-temperature process and an equivalent process. For this reason, the problem of diffusion of a damage or an impurity does not arise.

[0017] thus — this invention — a substrate — RTA — it changed into the condition of being easy to remove the natural oxidation film on the front face of a substrate by carrying out a short-time temperature up using law, and the natural oxidation film is physically removed by irradiating beams, such as Si of the constituent of a substrate, in this condition. Thus, impurity residue can be made hard to produce on a processing front face, since the beam of the constituent of a substrate is irradiated. Since it will not be impurities, such as F in the case of being based on etching, such as the conventional F, even if the atoms (Si etc.) of a substrate constituent remain in a processing front face, even if it heat-treats membrane formation annealing etc. after that, there is almost no bad influence. And it can be made hard to enter the damage on a front face of processing like [since the beam exposure has removed the natural oxidation film which changed into the condition of a temperature up being carried out and being easy to remove / in the case of being based on the conventional etching]. And it can be made hard to produce rather than the case where it is based on the elevated-temperature time amount at the conventional furnace, since a short-time substrate temperature up can be managed by the RTA method.

[0018] In addition, it cannot be overemphasized only by carrying out the short-time temperature up of the substrate by the RTA method that the natural oxidation film is unremovable. Moreover, it cannot be overemphasized that the natural oxidation film is unremovable only by Si accumulating only by carrying out a beam exposure to a substrate if it is Si beam in ordinary temperature, for example.

[0019]

[Example] (Example 1) Drawing 2 is the schematic diagram showing the configuration of the multi chamber equipment which **(ed) in the example 1 of this invention. In drawing 2 R> 2, each chamber is held at an ultra-high vacuum or a high vacuum, and is divided with the gate valve 1. It consists of the CVD room 2, the spatter rooms 3 and 4, an anteroom 5, and a UHV (ultra high vacuum, ultra-high vacuum) processing room 6, and, as for a chamber, a wafer can move now centering on an anteroom 5 between each chamber.

[0020] next, the UHV processing interior of a room where drawing 3 is held at the ultra-high vacuum of a 10-10 Torr base — it is the flat surface and cross-section schematic diagram showing the configuration of the surface treatment equipment currently installed in 6. In drawing 3 , 11 is a substrate electrode holder for holding a substrate 12, and this substrate electrode holder 11 is carrying out a configuration which faces across the edge of a substrate 12, and it is arranged so that substrate 12 front face may be downward suitable, so that the front face by the side of the component formation field of a substrate 12 and the rear face of this opposite side may not be covered. And it has the infrared lamp 13 as a heater which can irradiate infrared radiation from the flesh side of a substrate 12. Moreover, the molecular-beam cel 14 of 3x3 is arranged to the perpendicular direction of substrate 12 front face, and a molecular beam can be irradiated now on substrate 12 front face at homogeneity. Si of a high grade is charged by the molecular-beam cel 14.

[0021] First, the Si substrate 12 is moved to the UHV processing room 6 from the anteroom 5 currently maintained at the high vacuum. Subsequently, the Si substrate 12 is moved between an infrared lamp 13 and the molecular-beam cel 14, and it is substrate 12 skin temperature by the infrared lamp 13. It holds at 300 degrees C. The temperature of the molecular-beam cel 14 is raised to about 1400 degrees C between them, with the shutter shut. The temperature of this molecular-beam cel 14 is set up so that it may become [second] in about 1A /as a rate of the molecular-beam growth in substrate 12 front face. Then, substrate 12 skin temperature is raised, and the shutter of the molecular-beam cel 14 is opened for 15 seconds at the same time it amounts to 1000 degrees C. And substrate 12 temperature is dropped at the same time it closed the shutter of the

molecular-beam cel 14. Descent of substrate 12 temperature is in about 20 seconds so that temperature may not fall quickly. It lowers to 300 degrees C. Thereby, the dozens of A natural oxidation film of substrate 12 front face can be removed, and substrate 12 pure front face can be obtained. Here, the substrate skin temperature change to aging at the time of using this approach is shown in drawing 4 R> 4.

[0022] And the substrate 12 with which the clean surface was acquired is again returned to an anteroom 5, it moves to the CVD room 2, the spatter room 3, and the spatter room 4 respectively, and predetermined processing is added. As mentioned above, the semiconductor device which has the property which was excellent in this example since substrate 12 pure front face is obtained, there are no worries about contamination, it could be made to be able to move to the following chamber and the following predetermined processing was performed by adding the surface treatment equipment which can perform clean-surface processing extremely to the multi chamber equipment which consists of an ultra-high vacuum or a high vacuum was able to be manufactured. From the molecular-beam cel 14, since Si molecule beam of a high grade is irradiated, there is no impurity in addition to Si, and an impurity does not remain on a substrate 12. And since two or more molecular-beam cels 14 are used, a molecular beam is irradiated by the substrate 12 at homogeneity, and even when a 8 inch wafer is used, surface treatment can be performed uniformly. moreover, RTA according to an infrared lamp 13 in substrate 12 temperature up — since law is used, the time amount currently maintained at the elevated temperature is as short as about dozens of seconds, and diffusion of an impurity does not take place and does not have a damage, either.

[0023] (Example 2) This example is also explained to multi chamber equipment using the same thing as the equipment of an example 1. Drawing 5 is the flat surface and cross-section schematic diagram showing the configuration of the surface treatment equipment currently installed in the UHV processing room 6 which is a vacuum chamber of the vacuum devices held at the ultra-high vacuum of a 10-10 Torr base. In drawing 5 , the same sign as drawing 3 is carrying out the same or the cross-joint mold with which four substrates 12 can be held so that a considerable part may be shown, 11a may be a substrate electrode holder for holding a substrate 12 and substrate 12 front face may be downward suitable this substrate electrode-holder 11a, and rotates a core as a shaft. And under substrate electrode-holder 11a, it divides equally in the eight directions centering on a shaft, and is arranged from the anteroom 5 direction of drawing 2 in order of a loader 21, infrared lamp 13a, molecular-beam cel 14a, infrared lamp 13b, molecular-beam cel 14b, infrared lamp 13c, molecular-beam cel 14c, and an unloader 22. The infrared lamps 13a-13c here are arranged upward so that substrate 12 front face may be irradiated respectively. The molecular-beam cels 14a-14c are attached to one place, and are arranged 3x3, and it is made for a molecular beam to be irradiated by homogeneity on substrate 12 front face. Si of a high grade is charged by these molecular-beam cels 14a-14c. The unloader 22 has the composition that the substrate 12 which processing finished can be moved to an anteroom 5 so that a loader 21 can attach in substrate electrode-holder 11a of a cross-joint mold the substrate 12 which has moved from an anteroom 5.

[0024] First, a substrate 12 is moved to the UHV processing room 6 from the anteroom 5 currently maintained at the high vacuum. A substrate 12 is attached in substrate electrode-holder 11a with a loader 21 in that case. Subsequently, substrate electrode-holder 11a rotates, the substrate 12 attached in substrate electrode-holder 11a moves onto infrared lamp 13a, and substrate 12 skin temperature It is held at 300 degrees C. The temperature of molecular-beam cel 14a is raised to about 1400 degrees C between them. The temperature of this molecular-beam cel 14a is set up so that it may become [second] in about 1A /as a rate of the molecular-beam growth in substrate 12 front face. Substrate 12 front face is heated by 1200 degrees C on infrared lamp 13a. Shortly after substrate 12 skin temperature becomes 1200 degrees C, it will move onto molecular-beam cel 14a, and a molecular beam will be irradiated about 5 seconds, and a shutter closes. The following substrate 12 is attached in substrate electrode-holder 11a between them. If a shutter closes, a substrate 12 will move onto molecular-beam cel 14b. The substrate 12 following skin temperature If it becomes 300 degrees C, the front face of the first substrate 12 and the following substrate 12 will be heated by 1200 degrees C. If substrate 12 skin temperature becomes 1200 degrees C, it will move onto the following molecular-beam cel immediately, and a molecular beam will be irradiated about 5 seconds. This actuation is returned to the deed substrate 12 with a loader 21 by one rotation in an anteroom 5. The irradiation time of the molecular flow from the molecular-beam cels 14a-14c is set up as it has been total [of 10 seconds -] about 15 seconds. Moreover, substrate electrode-holder 11a of a cross-joint mold rotates so that each actuation may be suited. And if a substrate 12 goes round, the natural oxidation film of dozens of substrate 12 front face can be removed, and substrate 12 pure front face can be obtained. Here, the substrate skin temperature change to aging at the time of using this approach is shown in drawing 6 .

[0025] And the substrate 12 with which the clean surface was acquired is again returned to an anteroom 5, it moves to the CVD room 2, the spatter room 3, and the spatter room 4 respectively, and predetermined processing is added. As mentioned above, the semiconductor device which has the property which was excellent in this example since substrate 12 pure front face is obtained, there are no worries about contamination, it could be made to be able to move to the following chamber and the following predetermined processing was performed by adding the surface treatment equipment which can perform clean-surface processing extremely to the multi chamber equipment which consists of an ultra-high vacuum or a high vacuum was able to be manufactured. From the molecular-beam cels 14a-14c, since Si molecule beam of a high grade is irradiated, there is no impurity in addition to Si, and an impurity does not remain on a substrate 12. And since two or more molecular-beam cels are used, a molecular beam is irradiated by the substrate 12 at homogeneity, and even when a 8 inch wafer is used, surface treatment can be performed uniformly. And in this example, since infrared lamps 13a-13c and the molecular-beam cels 14a-14c can be arranged in by turns on a periphery and processing can be added to a substrate 12 one after another, surface treatment can be performed very efficiently. moreover, RTA according to infrared lamps 13-13c in substrate 12 temperature up — since law is used, the time amount currently maintained at the elevated temperature is as short as about dozens of seconds, and diffusion of an impurity does not take place and does not have a damage, either.

[0026]

[Effect of the Invention] According to this invention, in case the natural oxidation film of a processed substrate front face is removed, while being able to make impurity residue hard to produce on a processing front face, it can be made hard to go a damage into a processing front face, and impurity diffusion can be made hard to produce moreover and there is effectiveness of the ability to make degradation of a component property hard to produce.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] RTA of the case where the temperature up of the substrate is carried out using the conventional furnace, and this invention — it is drawing showing change of the substrate skin temperature to aging with the case where the temperature up of the substrate is carried out using law.
[Drawing 2] It is the schematic diagram showing the configuration of the multi chamber equipment which **(ed) in the example 1 of this invention.
[Drawing 3] It is the flat surface and cross-section schematic diagram showing the configuration of the surface treatment equipment which **(ed) in the example 1 of this invention.
[Drawing 4] It is drawing showing change of the substrate skin temperature to aging which **(ed) in the example 1 of this invention.
[Drawing 5] It is the flat surface and cross-section schematic diagram showing the configuration of the surface treatment equipment which **(ed) in the example 2 of this invention.
[Drawing 6] It is drawing showing change of the substrate skin temperature to aging which **(ed) in the example 2 of this invention.
[Drawing 7] The natural oxidation film on the front face of silicon is drawing showing the bad influence which it has on device basic structure.
[Description of Notations]
1 Gate Valve
2 CVD Room
3 Four Spatter room
5 Anteroom
6 UHV Processing Room
11 11a Substrate electrode holder
12 Substrate
13, 13a-13c Infrared lamp
14, 14a-14c Molecular-beam cel
21 Loader
22 Unloader

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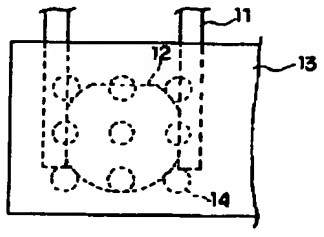
(54)【発明の名称】半導体装置の製造方法

(57)【要約】　(修正有)

【目的】　本発明は、半導体装置の製造方法に関し、被処理基板表面の自然酸化膜を除去する際、処理表面に不純物残渣を生じ難くすることができるとともに、処理表面にダメージを入り難くすることができ、しかも不純物拡散を生じ難くすることができ、素子特性の劣化を生じ難くすることができる半導体装置の製造方法を提供することを目的とする。

【構成】　被処理基板をＲＴＡ（Rapid Thermal Annealing)法により短時間加熱する加熱工程と、被処理基板に該被処理基板の構成物質のビームを照射するビーム照射工程とを同時に行うか、あるいは交互に少なくとも１回ずつ行うことにより、該被処理基板の表面処理を行う工程とを含むように構成する。

本発明の実施例１に則した表面処理装置の構成を示す平面及び断面概略図



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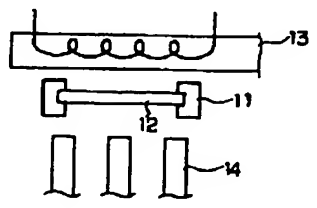

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【特許請求の範囲】

【請求項１】　被処理基板をＲＴＡ（Rapid Thermal Annealing）法により短時間加熱する加熱工程と、該被処理基板に該被処理基板の構成物質のビームを照射するビーム照射工程とを同時に行うか、あるいは交互に少なくとも１回ずつ行うことにより、該被処理基板の表面処理を行う工程とを含むことを特徴とする半導体装置の製造方法。

【請求項２】　前記ビーム照射は、複数の分子線セルにより行うことを特徴とする請求項１記載の半導体装置の製造方法。

【請求項３】　前記加熱は、赤外線照射加熱であることを特徴とする請求項１乃至２記載の半導体装置の製造方法。

【請求項４】　前記加熱工程と前記ビーム照射行程を同時に行う際は、前記赤外線照射加熱を前記被処理基板の素子形成領域の反対側の裏面から行い、該ビーム照射を該被処理基板の素子形成領域側の表面から行うことを特徴とする請求項３記載の半導体装置の製造方法。

【請求項５】　前記加熱工程と前記ビーム照射工程とを交互に行う際は、前記赤外線照射加熱と該ビーム照射工程とを前記被処理基板の素子形成領域側の面から行うことを特徴とする請求項３記載の半導体装置の製造方法。

【請求項６】　前記表面処理工程は、成膜前の前処理であることを特徴とする請求項５記載の半導体装置の製造方法。

【請求項７】　前記前処理は、複数のチャンバーを有するマルチチャンバー装置における前処理であることを特徴とする請求項６記載の半導体装置の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、半導体装置の製造方法に係り、詳しくは、半導体結晶製造技術及び電子デバイス製造プロセスに用いるシリコン等の基板の表面処理方法に適用することができ、特に、被処理基板の自然酸化膜を除去する際、処理表面に不純物残渣及びダメージ等を生じ難くして素子特性の劣化を生じ難くすることができる半導体装置の製造方法に関する。

【０００２】近年、２５６Ｍｂや１Ｇｂクラスのダイナミック等のＵＬＳＩ集積回路の実現に向けて、その基礎技術の開発研究が活発に行われている。そして、このクラスの集積回路では、最小加工寸法ルールが 0.3μm以下と極めて小さく、そのうえ各プロセスにおいては、低温化とともに高品質化が要求されている。しかも、素子の高集積化の要求に伴い、加工工程も大きく変わってきている。

【０００３】

【従来の技術】図７はシリコン表面の自然酸化膜がデバイス基本構造に与える悪影響を示す図である。図７（ａ）に示すように、シリコン基板31表面に自然酸化膜32が生じた状態でＳｉＯ₂絶縁膜33及びポリＳｉ配線層34を順次形成すると、ＳｉＯ₂絶縁膜33及びポリＳｉ配線層34内にガス、不純物等が拡散してＳｉＯ₂絶縁膜33及びポリＳｉ配線層34の膜質が悪くなり、耐圧不良等が生じ易くなる等素子特性が劣化し易くなる。

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【０００４】また、図７（ｂ）に示すように、シリコン基板31表面に自然酸化膜32が生じた状態でＳｉＯ₂絶縁膜33及びＡｌ配線層34を順次形成すると、、ＳｉＯ₂絶縁膜33及びＡｌ配線層34内にガス、不純物等が拡散してＳｉＯ₂絶縁膜33及びＡｌ配線層34の膜質が悪くなり、Ａｌ配線層34内に欠陥が誘起される等素子特性が劣化し易くなる。

【０００５】また、図７（ｃ）に示すように、ＳｉＯ₂絶縁膜33に形成された開口部33ａ内のシリコン基板31表面に自然酸化膜32が生じた状態でポリＳｉ配線層34を形成し、更にこのポリＳｉ配線層34表面に自然酸化膜が生じた状態でＳｉＮ絶縁膜35を形成すると、ポリＳｉ配線層34及びＳｉＮ絶縁膜35にガス、不純物等が拡散してポリＳｉ配線層34及びＳｉＮ絶縁膜35の膜質が悪くなり、シリコン基板31とポリＳｉ配線層34とでコンタクト不良が生じ易くなったり、キャパシタ容量が低下して不良が生じ易くなったりして素子特性が劣化し易くなる。この図７での問題は特に 0.3μmレベルのＵＬＳＩ集積回路等のプロセスで顕著になる。

【０００６】このように、自然酸化膜が生じた状態で次層を成膜してしまうと素子特性が劣化してしまうので、従来では、成膜する前に、アルゴンスパッタエッチングや水素プラズマエッチング、あるいはフッ素ラジカルエッチング等により表面処理して、自然酸化膜の汚れを除去していた。

【０００７】

【発明が解決しようとする課題】しかしながら、上記した従来の半導体装置の製造方法では、アルゴンスパッタエッチングや水素プラズマエッチング、あるいはフッ素ラジカルエッチング等により表面処理していたため、処理表面に水素、フッ素等の不純物が残留し易く、不純物が残留した状態で次層を成膜すると、成膜された膜内に上記不純物が拡散してしまい、その結果、成膜された膜の膜質が悪くなって素子特性が劣化し易いという問題があった。また、エッチングにより表面処理していたため、処理表面にダメージが入り易いという問題があった。表面にダメージが入ると、表面モホロジーが悪くなったり、また下地に拡散層があるような場合、拡散層までエッチングしてしまうことがあった。

【０００８】このため、処理表面に不純物が残留し、処理表面にダメージが入ってしまうという問題を解消するために、従来では、シリコン被処理基板を加熱炉を用いて約1000℃程度で高温加熱し、更にＳｉビームを十数秒照射することによりＳｉＯ₂自然酸化膜を除去する方法が知られている。なお、シリコン基板に前処理を行わず

SiO_2自然酸化膜の除去を行う場合は、基板温度を約1000℃にし、十数秒のＳｉビームを照射することにより清浄な基板表面を得ることができる。

【０００９】しかしながら、この方法では、1000℃という高温に基板温度を上げるのに、炉を用いて昇温していたため、昇温時間に長時間を要してしまう。このため、この長時間における高温保持のために、素子形成領域の拡散層等の不純物の拡散が生じてしまい、結局、上記したと同様不純物拡散に伴う素子特性が劣化してしまうという問題があった。

【００１０】そこで、本発明では、被処理基板表面の自然酸化膜を除去する際、処理表面に不純物残渣を生じ難くすることができるとともに、処理表面にダメージを入り難くすることができ、しかも不純物拡散を生じ難くすることができ、素子特性の劣化を生じ難くすることができる半導体装置の製造方法を提供することを目的としている。

【００１１】

【課題を解決するための手段】本発明による半導体装置の製造方法は上記目的達成のため、被処理基板をＲＴＡ(Rapid Thermal Annealing)法により短時間加熱する加熱工程と、該被処理基板に該被処理基板の構成物質のビームを照射するビーム照射工程とを同時に行うか、あるいは交互に少なくとも１回ずつ行うことにより、該被処理基板の表面処理を行う工程とを含むものである。

【００１２】本発明に係る被処理基板には、Ｓｉ、ＧａＡｓ、ＩｎＰ等の基板が挙げられ、これに対する被処理基板の構成物質のビームにはＳｉ、Ａｓ、Ｐ等のビームが挙げられる。また、ＲＴＡ法による加熱には、赤外線照射加熱等が挙げられる。本発明においては、前記ビーム照射は、複数の分子線セルにより行われる場合が好ましく、この場合、被処理基板に対して適宜均等に分布よく分子線セルを配置することで単一の分子線セルで行う場合よりも均等に分布よく被処理基板に照射することができる。

【００１３】本発明においては、加熱工程とビーム照射工程とを同時に行う際は、例えば赤外線照射線等の加熱を被処理基板裏面（素子形成領域と反対側の面）から行い、ビーム照射を被処理基板表面（素子形成領域側の面）から行うようにすればよく、また、加熱工程とビーム照射工程とを交互に行う際は、例えば赤外線照射等の加熱とビーム照射とを被処理基板表面から交互に行うようにすればよい。前者の場合は、後者の場合よりも装置システムを簡略化することができるとともに、容易に表面処理することができる。後者の場合は、両工程を被処理基板の表面側から行うことができるので、前者の場合よりも基板表面温度のばらつきを少なくすることができる。

【００１４】本発明においては、Ａｌ等の配線やSiO_2等の絶縁膜等の成膜前の前処理に好ましく適用させることができ、特に、ＣＶＤやスパッタ装置等、複数のチャンバーを有するマルチチャンバー装置における前処理工程に好ましく適用させることができる。

【００１５】

【作用】従来では、前述した如く、炉で基板温度を昇温していたため、図１（ａ）に示す如く、目的の温度である1000℃に達するまでに長時間を必要とし、実際には1000℃という温度を十数秒だけあれば自然酸化膜が除去できるにもかかわらず、数分から数十分という長時間の高温下に基板が曝されてしまうため、不純物の拡散やダメージがおこり実用上問題があった。

【００１６】これに対し、本発明では、ＲＴＡ法を用いるので、図１（ｂ）に示す如く、1000℃まで昇温するのに数秒程度あればよく、降温にも数秒から数十秒程度でよいので、基板を高温に保っている時間は従来の炉を用いる場合よりも極めて短くて済む。これは、不純物の拡散による影響が現れる前にプロセスを終わらせることができるので、低温プロセスと等価的プロセスであるといえる。このため、ダメージや不純物の拡散といった問題は起こらない。

【００１７】このように、本発明では、基板をＲＴＡ法を用いて短時間昇温することで基板表面の自然酸化膜を除去し易い状態にし、この状態で基板の構成物質のＳｉ等のビームを照射することで自然酸化膜を物理的に除去している。このように、基板の構成物質のビームを照射しているため、処理表面に不純物残渣を生じ難くすることができる。仮に、基板構成物質の原子（Ｓｉ等）が処理表面に残っても、従来のＦ等エッチングによる場合のＦ等のような不純物ではないので、その後、成膜アニール等の熱処理をしてもほとんど悪影響はない。そして、昇温されて除去し易い状態になった自然酸化膜をビーム照射によって除去しているため、従来のエッチングによる場合のような処理表面へのダメージを入り難くすることができる。しかも、ＲＴＡ法により短時間の基板昇温で済ませることができるため、従来の炉による高温時間による場合よりも生じ難くすることができる。

【００１８】なお、基板をＲＴＡ法で短時間昇温しただけでは、自然酸化膜を除去することはできないことは言うまでもない。また、基板にビーム照射しただけでは、例えば常温でのＳｉビームだと、Ｓｉが堆積されるだけで自然酸化膜を除去することはできないのは言うまでもない。

【００１９】

【実施例】（実施例１）図２は本発明の実施例１に則したマルチチャンバー装置の構成を示す概略図である。図２において、各々のチャンバーは超高真空あるいは高真空に保持され、ゲートバルブ１で仕切られている。チャンバーはＣＶＤ室２、スパッタ室３，４、準備室５及びＵＨＶ（ウルトラハイバキューム、超高真空）処理室６からなり、準備室５を中心として各チャンバー間をウエ

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ハが移動できるようになっている。

【００２０】次に、図３は10^{-10} Ｔｏｒｒ台の超高真空に保持されるＵＨＶ処理室内６に設置されている表面処理装置の構成を示す平面及び断面概略図である。図３において、11は基板12を保持するための基板ホルダーであり、この基板ホルダー11は基板12の素子形成領域側の表面及びこの反対側の裏面を覆うことのないように、基板12の縁を挟むような形状をしており、基板12表面が下に向くように配置されている。そして、基板12の裏から赤外線を照射することのできるヒーターとして赤外線ランプ13を備えている。また、基板12表面の垂直方向に３×３の分子線セル14が配置され、基板12表面に均一に分子線を照射できるようになっている。分子線セル14には、高純度のＳｉがチャージされている。

【００２１】まず、高真空に保たれている準備室５からＵＨＶ処理室６へＳｉ基板12を移動させる。次いで、Ｓｉ基板12を赤外線ランプ13と分子線セル14の間に移動し、赤外線ランプ13により基板12表面温度を 300℃に保持する。その間に分子線セル14の温度をシャッターを閉めたままで1400℃程度に上げておく。この分子線セル14の温度は、基板12表面における分子線成長のレートとして約１Å／秒になるように設定する。その後、基板12表面温度を上昇させ、1000℃に達すると同時に分子線セル14のシャッターを15秒間開ける。そして、分子線セル14のシャッターを閉じたと同時に基板12温度を下降させる。基板12温度の下降は急速に温度が下がることのないように20秒程度で 300℃まで下げる。これにより、基板12表面の数十Åの自然酸化膜を除去することができ、清浄な基板12表面を得ることができる。ここで、この方法を用いた場合の経時変化に対する基板表面温度変化を図４に示す。

【００２２】そして、清浄な表面が得られた基板12は再び準備室５に戻され、ＣＶＤ室２、スパッタ室３、スパッタ室４に各々移動し、所定の処理が加えられる。以上のように、本実施例では、超高真空または高真空からなるマルチチャンバー装置に極めて清浄な表面処理を行える表面処理装置を加えることによって、清浄な基板12表面が得られ、汚染の心配がなく、次のチャンバーに移動させ次の所定の処理を行うことができるので、優れた特性を有する半導体デバイスを製作することができた。分子線セル14からは高純度のＳｉ分子ビームが照射されるため、Ｓｉ以外に不純物がなく、基板12上に不純物が残存することもない。そして、分子線セル14を複数個用いているため、基板12に均一に分子線が照射され、８インチウエハを用いた場合でもむらなく表面処理が行える。また、基板12昇温には赤外線ランプ13によるＲＴＡ法を用いているため、高温に保っている時間は数十秒程度と短く、不純物の拡散は起こらず、ダメージもない。

【００２３】（実施例２）本実施例でも、マルチチャンバー装置には実施例１の装置と同一のものを用いて説明

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する。図５は10^{-10} Ｔｏｒｒ台の超高真空に保持される真空装置の真空室であるＵＨＶ処理室６内に設置されている表面処理装置の構成を示す平面及び断面概略図である。図５において、図３と同一符号は同一または相当部分を示し、11ａは基板12を保持するための基板ホルダーであり、この基板ホルダー11ａは、基板12表面が下に向くように基板12を４枚保持できる十字型をしており、中心を軸として回転するようになっている。そして、基板ホルダー11ａ下には、軸を中心に８方向に等分し、図２の準備室５方向からローダー21、赤外線ランプ13ａ、分子線セル14ａ、赤外線ランプ13ｂ、分子線セル14ｂ、赤外線ランプ13ｃ、分子線セル14ｃ、アンローダー22の順に配置されている。ここでの赤外線ランプ13ａ～13ｃは、各々基板12表面を照射するように上向きに配置されている。分子線セル14ａ～14ｃは１ヵ所に付き３×３本配置し、基板12表面に均一に分子線が照射されるようにする。この分子線セル14ａ～14ｃには、高純度のＳｉがチャージされている。ローダー21は、準備室５から移動してきた基板12を十字型の基板ホルダー11ａに取り付けることができるように、アンローダー22は、処理の終わった基板12を準備室５に移動させることができるような構成になっている。

【００２４】まず、高真空に保たれている準備室５からＵＨＶ処理室６へ基板12を移動させる。その際、基板12はローダー21により基板ホルダー11ａに取り付けられる。次いで、基板ホルダー11ａに取り付けられた基板12は、基板ホルダー11ａが回転し赤外線ランプ13ａ上に移動して基板12表面温度が 300℃に保持される。その間に分子線セル14ａの温度を1400℃程度に上げておく。この分子線セル14ａの温度は、基板12表面における分子線成長のレートとして約１Å／秒になるように設定する。基板12表面は赤外線ランプ13ａ上で1200℃に加熱される。基板12表面温度が1200℃になるとすぐに分子線セル14ａ上に移動し分子線が５秒程度照射され、シャッターが閉じる。その間に次の基板12が基板ホルダー11ａに取り付けられる。シャッターが閉じると基板12は分子線セル14ｂ上に移動する。次の基板12表面温度が 300℃になると、最初の基板12及び次の基板12の表面が1200℃に加熱される。基板12表面温度が1200℃になると、すぐに次の分子線セル上に移動し、分子線が５秒程度照射される。この操作を１回転分行い基板12はローダー21により準備室５に戻される。分子線セル14ａ～14ｃからの分子流の照射時間は合計10秒～15秒程度になるように設定されている。また、十字型の基板ホルダー11ａは各々の動作に合うように回転する。そして、基板12が一回りすると、基板12表面の数十の自然酸化膜を除去することができ、清浄な基板12表面を得ることができる。ここで、この方法を用いた場合の経時変化に対する基板表面温度変化を図６に示す。

【００２５】そして、清浄な表面が得られた基板12は再

び準備室５に戻され、ＣＶＤ室２、スパッタ室３、スパッタ室４に各々移動し、所定の処理が加えられる。以上のように、本実施例では、超高真空または、高真空からなるマルチチャンバー装置に極めて清浄な表面処理を行える表面処理装置を加えることによって、清浄な基板12表面が得られ、汚染の心配がなく、次のチャンバーに移動させ次の所定の処理を行うことができるので、優れた特性を有する半導体デバイスを製作することができた。分子線セル14ａ～14ｃからは高純度のＳｉ分子ビームが照射されるため、Ｓｉ以外に不純物がなく、基板12上に不純物が残存することもない。そして、分子線セルを複数個用いているため、基板12に均一に分子線が照射され、８インチウエハを用いた場合でもむらなく表面処理が行える。そして、本実施例では、円周上に赤外線ランプ13ａ～13ｃと分子線セル14ａ～14ｃを交互に並べ次々と基板12に処理を加えることができるので、極めて効率的に表面処理を行うことができる。また、基板12昇温には赤外線ランプ13～13ｃによるＲＴＡ法を用いているため、高温に保っている時間は数十秒程度と短く、不純物の拡散は起こらず、ダメージもない。

【００２６】

【発明の効果】本発明によれば、被処理基板表面の自然酸化膜を除去する際、処理表面に不純物残渣を生じ難くすることができるとともに、処理表面にダメージを入り難くすることができ、しかも不純物拡散を生じ難くすることができ、素子特性の劣化を生じ難くすることができるという効果がある。

【図面の簡単な説明】

【図１】従来の炉を用いて基板を昇温した場合と本発明のＲＴＡ法を用いて基板を昇温した場合との経時変化に対する基板表面温度の変化を示す図である。

【図２】本発明の実施例１に則したマルチチャンバー装置の構成を示す概略図である。

【図３】本発明の実施例１に則した表面処理装置の構成を示す平面及び断面概略図である。

【図４】本発明の実施例１に則した経時変化に対する基板表面温度の変化を示す図である。

【図５】本発明の実施例２に則した表面処理装置の構成を示す平面及び断面概略図である。

【図６】本発明の実施例２に則した経時変化に対する基板表面温度の変化を示す図である。

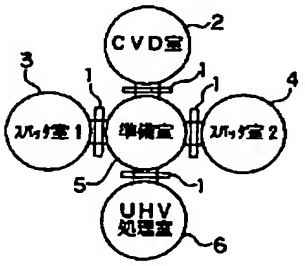
【図７】シリコン表面の自然酸化膜がデバイス基本構造に与える悪影響を示す図である。

【符号の説明】

1　ゲートバルブ
2　ＣＶＤ室
3，４　スパッタ室
5　準備室
6　ＵＨＶ処理室
11，11ａ　基板ホルダー
12　基板
13，13ａ～13ｃ　赤外線ランプ
14，14ａ～14ｃ　分子線セル
21　ローダー
22　アンローダー

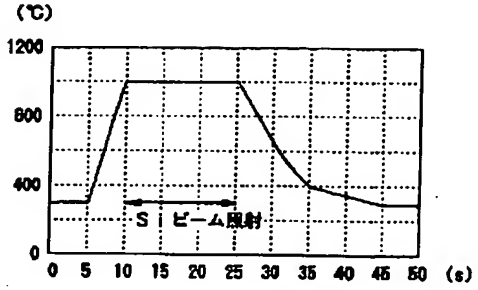
【図２】

本発明の実施例1に則したマルチチャンバー装置の構成を示す概略図



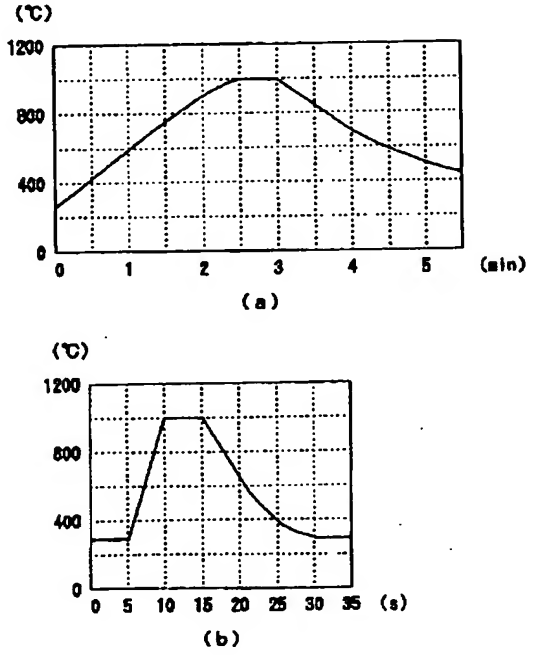
【図４】

本発明の実施例１に則した経時変化に対する基板表面温度の変化を示す図



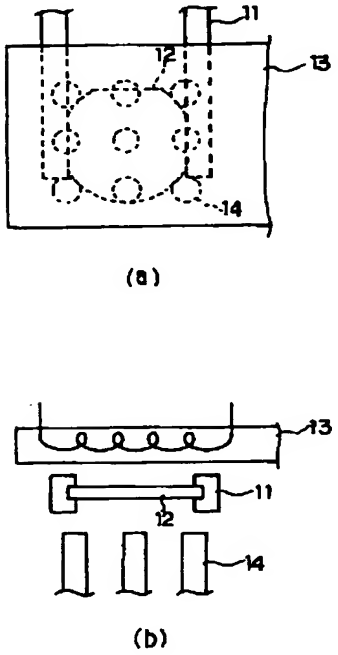
【図１】

従来の炉を用いて基板を昇温した場合と本発明のＲＴＡ法を用いて基板を昇温した場合との経時変化に対する基板表面温度の変化を示す図



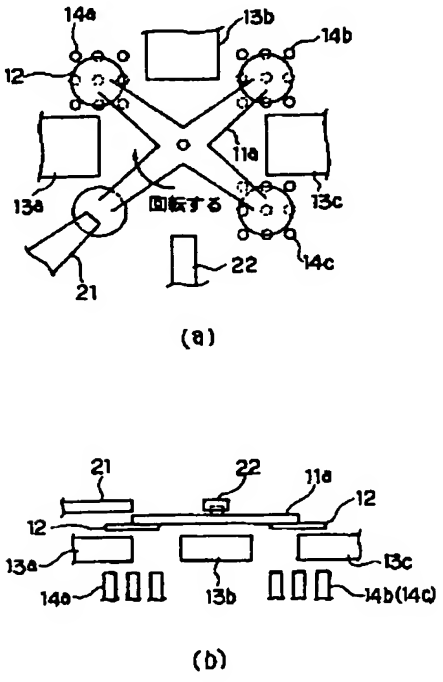
【図３】

本発明の実施例１に則した表面処理装置の構成を示す平面及び断面概略図



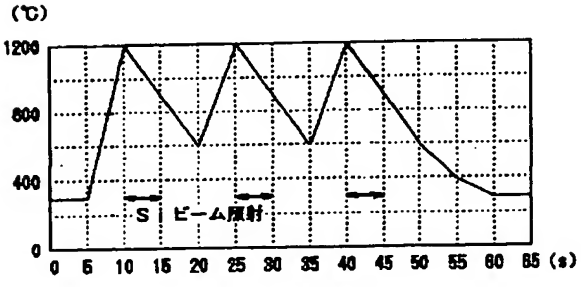
【図５】

本発明の実施例２に則した表面処理装置の構成を示す平面及び断面概略図



【図６】

本発明の実施例２に則した経時変化に対する基板表面温度の変化を示す図



【図７】

シリコン表面の自然酸化膜がデバイス基本構造に与える悪影響を示す図